PRELIMINARY

1/4 DUTY LCD DRIVER

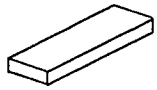
■ GENERAL DESCRIPTION

The NJU6437 is a 1/4 duty LCD driver for segment type LCD panel.

The LCD driver consists of 4-common and 32-segment drives up to 128 segments.

The rectangle outline is useful the COG applications.

■ PACKAGE OUTLINE



NJU6437C

■ FEATURES

- 32 Segment Drivers
- Duty and Bias Ratio : 1/4Duty, 1/3Bias(up to 128 segments)
- Serial Data Transmission (Shift Clock 2MHz max.)
- Oscillation Circuit On-chip
- Display Off Function (INH Terminal)
- Operating Voltage --- 2.4~3.6V
- LCD Driving Voltage --- 6.0V Max.
- Package Outline --- Chip / Bumped Chip
- C-MOS Technology

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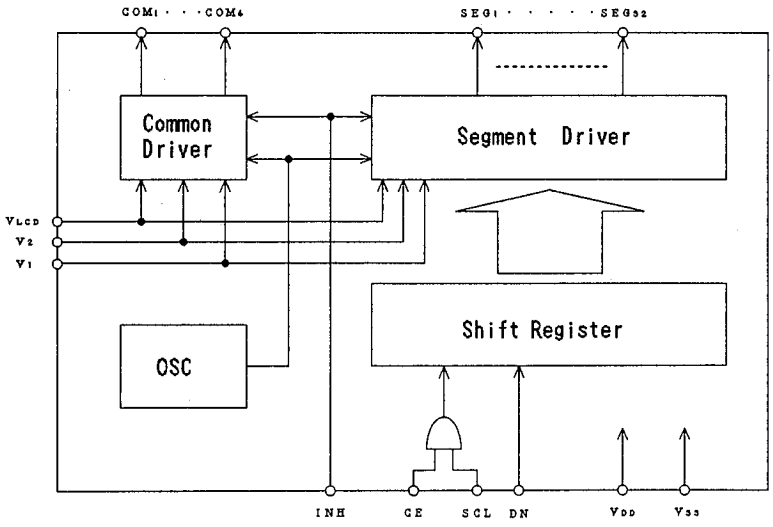
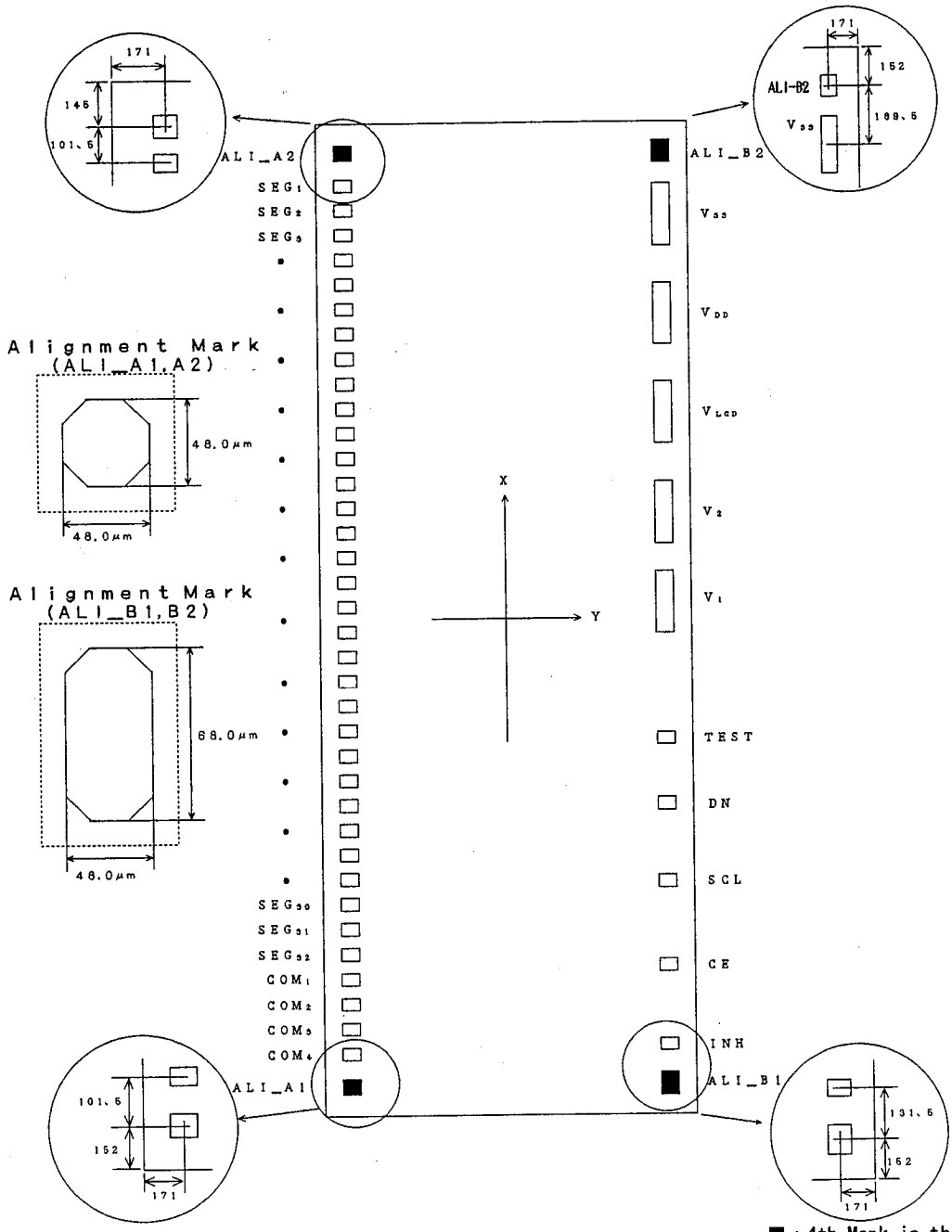
■ BLOCK DIAGRAM



■ PAD LOCATION



Chip size : 4.0mm x 1.5mm
Chip center : X=0μm, Y=0μm
Chip thickness : 400±30μm
Pad size : 50μm x 70μm
V_1, V_2, V_{LCD}, V_{DD}, V_{SS} Terminal is 250μm x 70μm
Bump height : 25umTYP.
Bump material : Au

■ : 4th Mark is the Alighment Mark.
The Alighment Mark is useful the COG Assembly.

■ PAD COORDINATES

Chip Size 4.0x1.5mm(Chip Center X=0μm, Y=0μm)

No	PAD NAME	X=(μm)	Y=(μm)	No	PAD NAME	X=(μm)	Y=(μm)
1	INH	-1716.5	-575.0	26	SEG_{16}	253.5	579.0
2	CE	-1406.5	-575.0	27	SEG_{17}	153.5	579.0
3	SCL	-1076.5	-575.0	28	SEG_{18}	53.5	579.0
4	DN	-766.5	-575.0	29	SEG_{19}	-46.5	579.0
5	TEST	-485.0	-575.0	30	SEG_{20}	-146.5	579.0
6	V_1	100.0	-575.0	31	SEG_{21}	-246.5	579.0
7	V_2	458.5	-575.0	32	SEG_{22}	-346.5	579.0
8	V_{LCD}	858.5	-575.0	33	SEG_{23}	-446.5	579.0
9	V_{DD}	1258.5	-575.0	34	SEG_{24}	-546.5	579.0
10	V_{SS}	1658.5	-575.0	35	SEG_{25}	-646.5	579.0
11	SEG_1	1753.5	579.0	36	SEG_{26}	-746.5	579.0
12	SEG_2	1653.5	579.0	37	SEG_{27}	-846.5	579.0
13	SEG_3	1553.5	579.0	38	SEG_{28}	-946.5	579.0
14	SEG_4	1453.5	579.0	39	SEG_{29}	-1046.5	579.0
15	SEG_5	1353.5	579.0	40	SEG_{30}	-1146.5	579.0
16	SEG_6	1253.5	579.0	41	SEG_{31}	-1246.5	579.0
17	SEG_7	1153.5	579.0	42	SEG_{32}	-1346.5	579.0
18	SEG_8	1053.5	579.0	43	COM_1	-1446.5	579.0
19	SEG_9	953.5	579.0	44	COM_2	-1546.5	579.0
20	SEG_{10}	853.5	579.0	45	COM_3	-1646.5	579.0
21	SEG_{11}	753.5	579.0	46	COM_4	-1746.5	579.0
22	SEG_{12}	653.5	579.0	ALIGNMENT	ALI_A1	-1848.0	579.0
23	SEG_{13}	553.5	579.0	ALIGNMENT	ALI_A2	1855.0	579.0
24	SEG_{14}	453.5	579.0	ALIGNMENT	ALI_B1	-1848.0	-579.0
25	SEG_{15}	353.5	579.0	ALIGNMENT	ALI_B2	1848.0	-579.0

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■ TERMINAL DESCRIPTION

NO.	SYMBOL	F U N C T I O N
1	INH	Display-Off Control Terminal : When display goes to off, the before display Off data in the shift-register is retained. "H" : Display-Off "L" : Display-On
2	CE	Chip Enable Signal Input Terminal : "H" : LCD display data "L" : Disable
3	SCL	Serial Data Transmission Clock Input Terminal : LCD display data are input synchronized SCL clock signal rise edge.
4	DN	Serial Data Input Terminal Data input timing : SCL clock rise edge
6	V_1	LCD Driving Voltage Adjust Terminal
7	V_2	LCD Driving Voltage Adjust Terminal
8	V_{LCD}	Power Supply for LCD Driving
9	V_{DD}	Power Supply (+3V)
10	V_{SS}	Power Supply (0V)
11~42	SEG_1 ~ SEG_{32}	LCD Segment Output Terminals
43~46	COM_1 ~ COM_4	LCD Common Output Terminals

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■ FUNCTIONAL DESCRIPTION

(1) Operation of each block

(1-1) Oscillation Circuit :

This circuits supply the basical clock signal to other circuits like as common driver and segment driver.

(1-2) Shift-Register

When the CE terminal is "H" (Enable mode), the display data is transferred to the shift-register synchronized by the shift clock on the SCL terminal.

(1-3) Common Divider Circuit

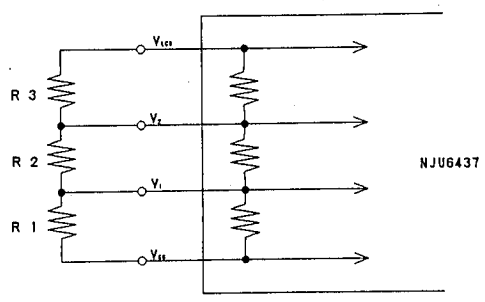
This circuit divides the oscillating signal to generate the common timing.

(1-4) Segment Divider Circuit

This circuit divides the oscillating signal to generate the segment timing.

(1-5) The LCD Driving Voltage Adjust circuit

The incorporated Bleeder Resistance sets 1/3 bias, and LCD Driver ability can be increased by connecting external resistance.



(2) Display Data input timing, correspond to segment and common terminal

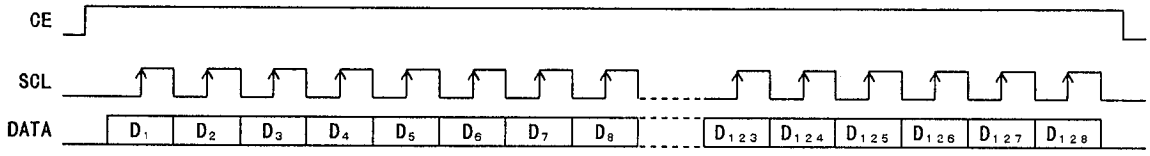
When the CE terminal is "H" (Enable mode), the display data is transferred to the shift-register synchronized by the shift clock on the SCL terminal.
When the power is turned on, whole data in the shift-resister are "L".

※ Whole 128bits data transfer to the shift register. When the input data in less than 128 bits, parts which bit data is inputed corresponded to display, and segment which correspond to the rest part in "off".
In care of over then 128bits, front 128bits from fall edge of "CE" signal is valid.

・Input data correspond to Segment Status
The "H" input data correspond to segment "ON" and "L" correspond to "OFF".

Data (D1···D128)	Segment Status
"H"	ON
"L"	OFF

・Display Data Correspond to Segment Status



(2-3) Display Data Correspond to Segment and Common Terminals

Segment	Data	COM_1	COM_2	COM_3	COM_4
SEG_1	D_1 D_2 D_3 D_4	○	○	○	○
SEG_2	D_5 D_6 D_7 D_8	○	○	○	○
⋮	⋮	⋮	⋮	⋮	⋮
SEG_{31}	D_{121} D_{122} D_{123} D_{124}	○	○	○	○
SEG_{32}	D_{125} D_{126} D_{127} D_{128}	○	○	○	○

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Operating Voltage (1)	V_{DD}	-0.3 ~ +7.0	V
Operating Voltage (2)	V_{LCD}	-0.3 ~ +7.0	V
Operating Voltage (3)	V_1, V_2	-0.3 ~ +7.0	V
Input Voltage	V_{IN}	-0.3 ~ VDD	V
Operating Temperature	T_{opr}	-20 ~ +75	°C
Storage Temperature	T_{stg}	-55 ~ +125	°C

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2) All voltage values are specified as V_{SS} = 0 V

Note 3) The relation: $V_{LCD} \geqq V_2 \geqq V_1 \geqq V_{SS}$ must be maintained.

Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation.

■ ELECTRICAL CHARACTERISTICS

· DC Characteristics

(Ta=25°C, V_{DD}=3.0~5.0V, V_{SS}=0V, V_{LCD}=6.0V)

PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	NOTE
Operating Voltage(1)	Recommend	V_{DD}	V_{DD} Terminal		2.4	3.0	3.6	V	
	Available	V_{DD}	V_{DD} Terminal		2.4	3.0	5.5	V	
Operating Voltage (2)		V_{LCD}	V_{LCD} Terminal		2.0		6.0	V	
Operating Voltage (3)		V_2	V_2 Terminal		2.0	$2/3V_{LCD}$	V_{LCD}	V	
Operating Voltage (4)		V_1	V_1 Terminal		0.7	$1/3V_{LCD}$	V_2	V	
"H" Input Voltage		V_{IH}	CE, SCL, DN, INH Terminals		$0.7V_{DD}$		V_{DD}	V	
"L" Input Voltage		V_{IL}	CE, SCL, DN, INH Terminals		V_{SS}		$0.3V_{DD}$	V	
"H" Input Current		I_{IH}	CE, SCL, DN, INH Term., $V_{IN}=V_{DD}$				5	μA	
"L" Input Current		I_{IL}	CE, SCL, DN, INH Term., $V_{IN}=V_{SS}$				5	μA	
"H" Output Voltage(1)		$V_{OH(1)}$	$SEG_1 \sim SEG_{32}$ Term., I_O= -1μA		V_{LCD}-0.6			V	5
"L" Output Voltage(1)		$V_{OL(1)}$	$SEG_1 \sim SEG_{32}$ Term., I_O= 1μA				V_{DD}+0.6	V	5
Middle Level Voltage 1/3 (1)		$V_{MS1/3}$	$SEG_1 \sim SEG_{32}$ Term., I_O= ±1μA		$1/3V_{LCD}$ -0.6	$1/3V_{LCD}$	$1/3V_{LCD}$ +0.6	V	5
Middle Level Voltage 2/3 (1)		$V_{MS2/3}$	$SEG_1 \sim SEG_{32}$ Term., I_O= ±1μA		$2/3V_{LCD}$ -0.6	$2/3V_{LCD}$	$2/3V_{LCD}$ +0.6	V	5
"H" Output Voltage(2)		$V_{OH(2)}$	$COM_1 \sim COM_4$ Term., I_O= -30μA		V_{LCD}-0.6			V	6
"L" Output Voltage(2)		$V_{OL(2)}$	$COM_1 \sim COM_4$ Term., I_O= 30μA				V_{SS}+0.6	V	6
Middle Level Voltage 1/3 (2)		$V_{MC1/3}$	$COM_1 \sim COM_4$ Term., I_O= ±1μA		$1/3V_{LCD}$ -0.6	$1/3V_{LCD}$	$1/3V_{LCD}$ +0.6	V	6
Middle Level Voltage 2/3 (2)		$V_{MC2/3}$	$COM_1 \sim COM_4$ Term., I_O= ±1μA		$2/3V_{LCD}$ -0.6	$2/3V_{LCD}$	$2/3V_{LCD}$ +0.6	V	6
Operating Current (1)		I_{SS}	V_{DD} Terminal	V_{DD}=5.0V V_{LCD} OPEN		16	30	μA	
				V_{DD}=3.0V V_{LCD} OPEN		7.5	10		
Operating Current (2)		I_{LCD}	V_{LCD} Terminal	V_{DD}=3.0V V_{LCD}=6.0V			12	μA	
Hysteresis Voltage		V_H	CE, SCL, DN, INH Terminal	V_{DD}=5.0V	0.3	0.6		V	
				V_{DD}=3.0V	0.3	1.0			

(Note 5) Segment terminals are open.

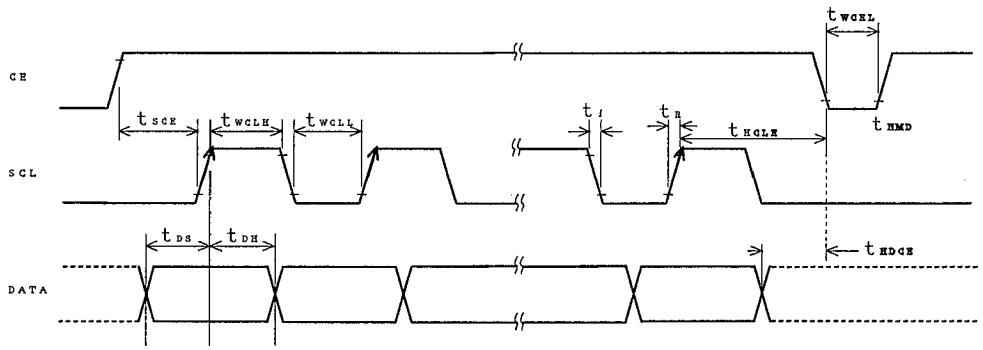
(Note 6) Common terminals are open.

・AC Characteristics

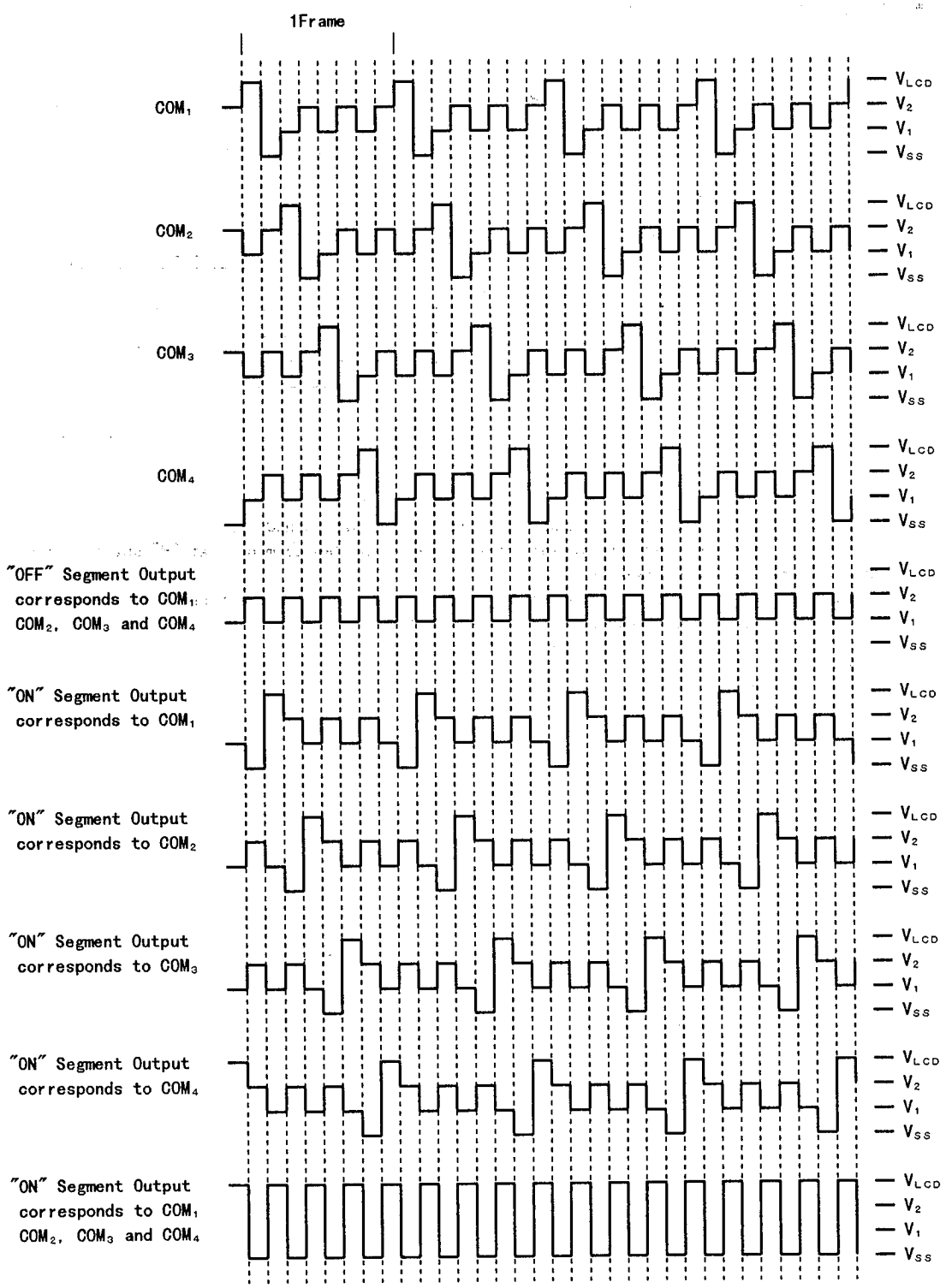
(Ta=25°C, V_{DD}=3.0V, V_{SS}=0V, V_{LCD}=6.0V)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
"L" Clock Pulse Width	t_{WCLL}	SCL		0.25	—	—	μs
"H" Clock Pulse Width	t_{WCLH}	SCL		0.25	—	—	μs
SCL Rise time, Fall time	t_r, t_f	SCL		—	—	50	ns
Data Set-up Time	t_{DS}	DN, SCL		0.25	—	—	μs
Data Hold Time	t_{DH}	SCL		0.25	—	—	μs
CE Set-up Time	t_{SCE}	CE, DN		1.25	—	—	μs
CE Hold Time	t_{HCLE}	SCL, CE		1.00	—	—	μs
"L" CE Pulse Width	t_{WCEL}	CE		4.00	—	—	μs
Frame Frequency	f_O	COM_1～COM_4,	V_{DD}=5.0V	45	75	—	Hz
		SEG_1～SEG_{32}	V_{DD}=3.0V	45	70	—	

・Input Timing Characteristics



■ LCD Driving Waveform(1/4DUTY・1/3BIAS)



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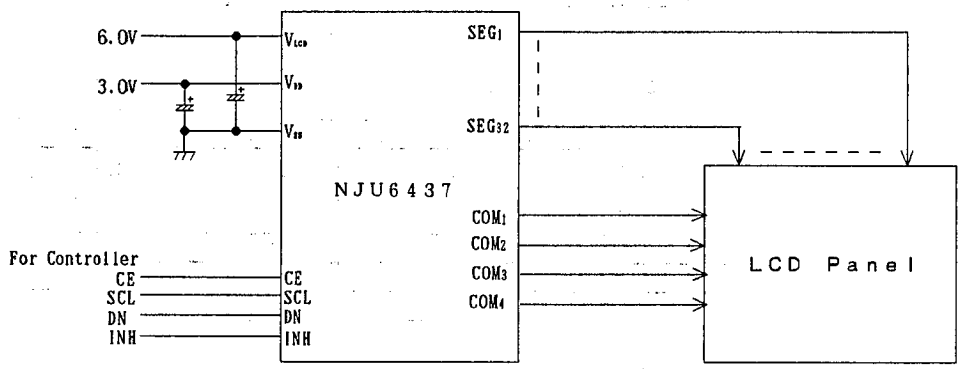
■ APPLICATION CIRCUIT



(Note) The internal display data is undefined when V_{DD} is just turned on.
To avoid the meaningless display, please keep the INH terminal at "H" until proper display data has been transferred.
In order to set the initial condition, 128-bit blank data or the first 128-bit data to be displayed should be transferred.

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MEMO